So $C\subseteq I$. Conversely, let us take $\sum_{j=1}^{6}\eta_j l_j(x)g_j(x)\in I$, where $l_j(x)\in R[x,\theta_i]/(x^n-1)$ for $j=1,2,3,4,5,6$, then $\eta_j l_j(x)=\eta_j k_j(x)$ for some $k_j(x)\in\mathbb{F}_q[x,\theta_i]$ for $j=1,2,\cdots,6$. Hence $I\subseteq C$. Therefore, $C=I$. Since $|C|=|C_1\|C_2\|C_3\|C_4\|C_5\|C_6|$, then we have $|C|=q^{6n-\sum_{j=1}^{6}deg(g_j(x))}$.

The next theorem shows that the skew cyclic codes over R are principally generated.

Theorem 3.3 Let $C_j=\langle g_j(x)\rangle$, where $g_j(x)$ are monic polynomials over $\mathbb{F}_q$ for $j=1,2,3,4,5,6$. Let C, expressed as (1), be a skew cyclic code over R, then there exists a unique polynomial $g(x)\in R[x,\theta_i]$ such that $C=\langle g(x)\rangle$ and $g(x)$ is a right divisor of x^n-1, where $g(x)=\sum_{j=1}^{6}\eta_j g_j(x)$.

Proof Let $g(x)=\sum_{j=1}^{6}\eta_j g_j(x)$, then it is easy to verify that $\langle g(x)\rangle\subseteq C$. Conversely, $\eta_j g_j(x)=\eta_j g(x)$, where $1\leqslant j\leqslant 6$, which implies that $C\subseteq\langle g(x)\rangle$. Thus $C=\langle g(x)\rangle$. Since $g_j(x)$ are monic right divisors of x^n-1 in $\mathbb{F}_q[x,\theta_i]$, then there are $h_j(x)$ in $\mathbb{F}_q[x,\theta_i]/(x^n-1)$ such that $x^n-1=h_i(x)g_i(x)$, $1\leqslant i\leqslant 6$. Thus $[2^{-1}\theta_i(2)(\eta_1 h_1(x)+\eta_2 h_2(x))+4^{-1}\theta_i(4)(\eta_3 h_3(x)+\eta_4 h_4(x)+\eta_5 h_5(x)+\eta_6 h_6(x))]\cdot g(x)=2^{-1}\theta_i(2)(\eta_1\theta_i(\eta_1)h_1(x)g_1(x)+\eta_2\theta_i(\eta_2)h_2(x)g_2(x))+4^{-1}\theta_i(4)(\eta_3\theta_i(\eta_3)h_3(x)g_3(x)+\eta_4\theta_i(\eta_4)h_4(x)g_4(x)+\eta_5\theta_i(\eta_5)h_5(x)g_5(x)+\eta_6\theta_i(\eta_6)h_6(x)g_6(x))=(\eta_1+\eta_2+\eta_3+\eta_4+\eta_5+\eta_6)(x^n-1)=x^n-1$. Hence $g(x)$ is a right divisor of x^n-1.

The following corollary is an immediate consequence of the above theorem.

Corollary 3.3 Every left submodule of $R[x,\theta_i]/(x^n-1)$ is principally generated.

Let $g(x)=\sum_{i=0}^{r}g_i x^i$ and $h(x)=\sum_{i=0}^{n-r}h_i x^i$ be polynomials in $\mathbb{F}_q[x,\theta_i]$ such that $x^n-1=h(x)g(x)$ and C be the skew cyclic code generated by $g(x)$ in $\mathbb{F}_q[x,\theta_i]/(x^n-1)$. Then the dual code of C is a skew cyclic code generated by the polynomial $\widetilde{H}(x)=h_{n-r}+\theta_i(h_{n-r-1})x+\cdots+\theta_i^{\,n-r}(h_0)x^{n-r}$ (see Ref.[5], Corollary 18). We are now ready to prove the following corollary for the generator polynomial and the cardinality of the dual code of a skew cyclic code over R.

Corollary 3.4 Let $C_j=\langle g_j(x)\rangle$ be skew cyclic codes over $\mathbb{F}_q$, where $x^n-1=h_j(x)g_j(x)$ in $\mathbb{F}_q[x,\theta_i]$ for $j=1,2,\cdots,6$. If $C=\eta_1C_1\oplus\eta_2C_2\oplus\eta_3C_3\oplus\eta_4C_4\oplus\eta_5C_5\oplus\eta_6C_6$, then $C^{\perp}=\langle h(x)\rangle$, where $h(x)=\sum_{j=1}^{6}\eta_j\tilde{h}_j(x)$ and $|C^{\perp}|=q^{\sum_{j=1}^{6}\deg(g_j(x))}$.

Proof By Theorem 2.1, we have $C^{\perp}=\eta_1C_1^{\perp}\oplus\eta_2C_2^{\perp}\oplus\eta_3C_3^{\perp}\oplus\eta_4C_4^{\perp}\oplus\eta_5C_5^{\perp}\oplus\eta_6C_6^{\perp}$. Since $C_j^{\perp}=\langle h_j(x)\rangle$ for $j=1,2,3,4,5,6$, we conclude by Theorem 3.3 that $C^{\perp}=\langle h(x)\rangle$.

In order to study the idempotent generators of skew cyclic codes over R, we need the following two lemmas which can be found in Ref.[9].

Lemma 3.2[9] Let $g(x)\in\mathbb{F}_q[x,\theta_i]$ be a monic right divisor of x^n-1. If $(n,t_i)=1$, then $g(x)\in\mathbb{F}_p[x,\theta_i]$, where $t_i=m/i$ denotes the order of the automorphism θ_i.

Lemma 3.3[9] Let $g(x)\in\mathbb{F}_q[x,\theta_i]$ be a monic right divisor of x^n-1 and $C=\langle g(x)\rangle$. If $(n,q)=1$ and $(n,t_i)=1$, then there exists an idempotent polynomial $e(x)\in\mathbb{F}_q[x,\theta_i]/(x^n-1)$ such that $C=\langle e(x)\rangle$.

Now, we give the idempotent generators of skew cyclic codes over R.

Corollary 3.5 Let $C=\eta_1C_1\oplus\eta_2C_2\oplus\eta_3C_3\oplus\eta_4C_4\oplus\eta_5C_5\oplus\eta_6C_6$ be a skew cyclic code of length n over R and $(n,q)=1$, $(n,t_i)=1$. Then C_i has the idempotent generators $e_i(x)$, $i=1,2,3,4,5,6$. Moreover, $e(x)=\eta_1e_1(x)+\eta_2e_2(x)+\eta_3e_3(x)+\eta_4e_4(x)+\eta_5e_5(x)+\eta_6e_6(x)$ is an idempotent generator of C, that is, $C=\langle e(x)\rangle$.

Proof In the light of Theorem 3.3 and Lemma 3.3, the proof follows.

The following theorem gives the number of skew cyclic codes of length n over R.

Theorem 3.4 Let $(n,t_i)=1$ and $x^n-1=\prod_{i=1}^{r}p_i^{s_i}(x)$ where $p_i(x)\in\mathbb{F}_q[x,\theta_i]$ is irreducible. Then the number of skew cyclic codes of length n over R is $\prod_{i=1}^{r}(s_i+1)^6$.

Proof In view of Lemma 3.2, if $(n,t_i)=1$, then $p_i(x) \in \mathbb{F}_p[x, \theta_i]$. In this case the number of skew cyclic codes of length n over $\mathbb{F}_q$ is $\prod_{i=1}^{r}(s_i+1)$. Since $C=\eta_1 C_1 \oplus \eta_2 C_2 \oplus \eta_3 C_3 \oplus \eta_4 C_4 \oplus \eta_5 C_5 \oplus \eta_6 C_6$, then $\prod_{i=1}^{r}(s_i+1)^6$ is the number of skewcyclic codes of length n over R.

Note that when $(n, t_i) \neq 1$ in Theorem 3.4, the factorization of x^n-1 is not unique in $\mathbb{F}_q[x, \theta_i]$, therefore we can not say anything certain about the number of skew cyclic codes in this case. Now, we conclude this section with the following example.

Example 3.1 Let γ be the generator of the multiplicative group of $\mathbb{F}_9$, where γ is a root of a primitive polynomial x^2+x+2 over $\mathbb{F}_3$. And θ be the Frobenius automorphism over $\mathbb{F}_9$, i.e. $\theta(\Lambda)=\Lambda^3$ for any $\Lambda \in \mathbb{F}_9$. Then $x^6-1=(2+(2+\gamma)x+(1+2\gamma)x^3+x^4)(1+(2+\gamma)x+x^2)=(2+x+(2+2\gamma)x^2+x^3)(1+x+2\gamma x^2+x^3) \in \mathbb{F}_9[x, \theta]$. Let $g_1(x)=g_2(x)=g_3(x)=2+(2+\gamma)x+(1+2\gamma)x^3+x^4$ and $g_4(x)=g_5(x)=g_6(x)=2+x+(2+2\gamma)x^2+x^3$, then $C_1=\langle g_1(x)\rangle$, $C_2=\langle g_2(x)\rangle$ and $C_3=\langle g_3(x)\rangle$ are skew cyclic codes of length 6 over $\mathbb{F}_9$ with dimensions 4; $C_4=\langle g_4(x)\rangle$, $C_5=\langle g_5(x)\rangle$ and $C_6=\langle g_6(x)\rangle$ are skew cyclic codes of length 6 over $\mathbb{F}_9$ with dimensions 3. Also if we take $g(x)=\eta_1 g_1(x)+\eta_2 g_2(x)+\eta_3 g_3(x)+\eta_4 g_4(x)+\eta_5 g_5(x)+\eta_6 g_6(x)$, then C is a skew cyclic code of length 6 over $\mathbb{F}_9+u\mathbb{F}_9+v\mathbb{F}_9+uv\mathbb{F}_9+v^2\mathbb{F}_9+uv^2\mathbb{F}_9$. Thus the Gray image $\Phi(C)$ of C is a $[36, 21, 4]$ code over $\mathbb{F}_9$.

4 Conclusion

In this paper, we studied the structural properties of skew cyclic codes over the ring $R=\mathbb{F}_q+u\mathbb{F}_q+v\mathbb{F}_q+uv\mathbb{F}_q+v^2\mathbb{F}_q+uv^2\mathbb{F}_q$ by taking the automorphism θ_i. We proved that the gray image of a skew cyclic code of length n over R was a skew 6-quasi cyclic code of length $3n$ over $\mathbb{F}_q$. It was also shown that skew cyclic codes over R were principally generated. Further, we obtained idempotent generators of skew cyclic codes over R. Last, we gave the number of skew cyclic codes of length n over R under certain conditions. Note that this paper included Ref. [10-11] as special cases, because rings in Ref. [10-11] are subrings of the ring R in this paper.

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一种变粒度的闪存地址映射方案

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摘要:闪存转换层最重要的功能是地址映射.地址映射需要同时具备高性能和低内存占用.基于需求的页级映射方案DFTL能有效节约内存且具有页级映射方案特有的灵活性,但是这种方案中,每个缓存槽只能存储一条映射记录,当缓存大小一定时,缓存中的映射记录数量有限;此外,这种方案没有考虑到请求的空间局部性.因此这种方案中,缓存命中率较低,DFTL需要频繁访问闪存来读取映射记录,降低了系统性能.于是针对命中率低的问题,提出了一种基于需求的变粒度映射方案VGFTL.这种方案可显著提高缓存的命中率.实验表明,VGFTL缓存平均命中率达到89.85%,远高于DFTL的45.46%,块擦除次数以及平均响应时间这两项指标优于DFTL,其性能接近纯页级映射方案.

关键词:闪存;闪存转换层;地址映射;变粒度映射

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A variable granularity-based mapping scheme

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Abstract: Address mapping is the most important function of flash translation layer (FTL), and it should have both high performance and low memory footprint. Although demand-based address mapping scheme (DFTL) has relatively high performance and low memory footprint, it has problems. First, it is a page-level mapping scheme. Each cache slot stores only one mapping record, and each mapping record stores only one physical page number and the corresponding logical page number, so that the cache , at a fixed size, can only store a limited number of mapping records. Second, each mapping record itself cannot exploit the spatial locality of the request. Thus, in the DFTL scheme, since the cache hit ratio is low, DFTL has to frequently access the mapping pages in the flash memory to read the mapping records, which significantly reduces the performance of the system. A new scheme named VGFTL (a mapping scheme of variable granularity-based flash translation layer) was proposed, which could significantly increase the cache hit ratio. Experimental results show that the average hit ratio of cache has reached 89.85% in VGFTL scheme, which is much higher than that of the DFTL scheme, 45.46%. VGFTL can significantly

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reduce the number of block erasures and system response time compared to DFTL, and is close to pure page-level mapping scheme in performance.

Key words: NAND flash; flash translation layer; address mapping; variable granularity-based mapping

0 引言

闪存具有功耗低、发热小、重量轻、尺寸小等的优点.随着闪存容量瓶颈的突破、性能的优化以及成本的下降,闪存已经变成非常重要的数字存储介质.然而,闪存的异地更新、块擦写次数有限等特性使得现有的文件系统无法直接管理闪存.闪存存储系统一般使用闪存转换层(flash translation layer,FTL)将闪存模拟成传统块设备.地址映射是闪存转换层中最重要的功能,它使用映射记录保存供文件系统使用的逻辑地址和闪存上的物理地址之间的对应关系.为了实现快速寻址,全部或部分映射记录被缓存在内存中.因此,如何构建高效的地址映射方案并减少缓存对内存的占用成为一个重要问题.

闪存转换层目前主要使用三类地址映射方案[1]:纯页级映射[2]、块级映射[3-4]、混合映射[5].纯页级映射方案的地址映射单位为页,和闪存的读写单位一致,一个逻辑页可以映射到任意物理页,这种映射方案非常灵活,读写效率高,但是由于其映射粒度太小,导致映射表太大.块级映射的映射粒度大,以块为映射单位,逻辑地址包含逻辑块号和块内偏移量两个部分,映射表中只保存逻辑块到物理块之间的对应关系,内存占用小,但是这种映射方案不够灵活,更新数据前需要迁移块内多页数据并擦除块,性能很低.混合映射方案将大部分物理块作为数据块,用块级映射管理,少量物理块作为日志块用于存储更新数据,用页级映射管理.混合映射的映射表占用内存较小,但是带来了合并操作,因此性能不佳.

以上三种映射方案中.纯页级映射的性能最好,但是映射表占用内存大.为了解决这一问题,有学者提出了一种基于需求的页级映射方案(DFTL)[6],这种方案中,完整的映射表存储在闪存中的映射页中,而部分最新使用过的映射记录缓存在内存.DFTL 采用最近最少使用算法(LRU)作为缓存的置换策略.缓存大小可通过配置缓存槽(Slot)数量来决定.因此,DFTL 能有效减少内存占用并保持页级映射的高性能.但是被缓存的映射记录有限,导致 DFTL 需要频繁读写闪存来获取和回写映射记录,这些附加操作影响了 DFTL 的性能.

本文提出了一种基于需求的变粒度映射方案,这种方案的映射粒度不再是页,而是通过合并多条连续映射记录后产生的一条映射条目,缓存槽存储的是映射条目而非映射记录,因此其粒度大于或等于页,每个槽存储的映射条目所包含的页级映射记录数量不等.通过上述方式使得缓存中映射信息的存储密度大大增加,在缓存大小不变的前提下,增加了其中映射记录的数量,提高了缓存的命中率;另外,每条映射条目包含的都是逻辑地址上连续的多条映射记录,提高了系统的空间局部性能.实验结果表明:与 DFTL 相比,本文提出的方案在各种负载输入下,缓存的平均命中率达到 89.85%,远高于 DFTL 的 45.46%,块擦除次数以及平均响应时间这两项指标优于 DFTL,接近纯页级映射方案.

1 地址映射方案

NAND 型闪存由物理块组成,每个物理块由数量一定的物理页组成,块是擦除操作的基本单位,页是读写操作的基本单位.被擦除后的块被称为空闲块,其中的页被称为空闲页.

闪存有先擦后写的特性,即当物理页被写入数据后无法直接更新其中的数据,需要擦除该页所属的块后才能再次写入数据.我们期望闪存像磁盘一样采用本地更新,更新一页数据需要读取该页中所有有效数据并修改内容,然后擦除该页所在物理块,最后将修改后的多页数据回写到该块.由此可见,闪存的本地更新效率非常低下而且会造成物理块因被频繁擦写而快速老化.闪存更新数据采用异地更新,更新某个逻辑页的数据时,更新数据写入到其他空闲页中.异地更新方式造成管理闪存时必须采用地址映射机制记录逻辑地址到物理地址之间的对应关系.映射机制建立在映射表基础之上,为了加快寻址速度,映射表中全部或部分记录被缓存在内存中.

来自文件系统的逻辑地址通过地址映射被翻译成闪存中物理地址,地址映射方案根据映射粒度主要分 3 类:页级映射、块级映射和混合映射.

纯页级映射的映射粒度是页,和闪存的读写单