OMP 算法在 Gabor 字典上对信号进行分解.

正交匹配追踪算法的主要思路是在每一次匹配过程中,最后一次匹配得到的原子均需要与之前所得原子进行正交化,从而使得所有被匹配到的原子相互正交,构成正交基底,而通过再次迭代得到的原子则属于该正交基底张成空间的补空间.

本文提出的改进的 OMP 算法如表 2 所示,其中,观测向量 $f \in R^N$,字典矩阵 $\boldsymbol{D} \in R^{N\times M}$,$N$ 维重构信号 x 为输出结果.在算法的步骤 3,与经典 OMP 算法不同,由于构成核脉冲信号 $\hat{f}(t)=\sum_{j=1}^{J}\alpha_i g_j(t)$ 的 J 个原子的系数 α_i 需要保持一定比例关系,目标函数 $\min_\alpha \|\boldsymbol{y}-\boldsymbol{D}_n\boldsymbol{\alpha}\|_2$ 不再为凸函数,不能直接使用经典的最小二乘优化方法求解,本文采用遗传算法,通过少量的交叉、变异即可得到满意精度的解.

算法 2.2 改进的 OMP 算法

输入:稀疏字典矩阵 D,检测得到的核辐射脉冲向量 y

稀疏度 K;

输出:α 的稀疏逼近;

初始化:残差 $R0f=y$,索引集 $\Lambda_0=\varnothing$,$n=1$,D 由 K-SVD 学习得到;

迭代步骤 1—步骤 5:

步骤 1:求出 $R^{n-1}f$ 和矩阵 D 的每一列 d_j 的最大内积对应的脚标 λ_n,

$$\lambda_n=\mathrm{argmax}_{j=1,\cdots,M}|<d_{j-1},R^{n-1}f>|;$$

步骤 2:更新索引集 $\Lambda_n=\Lambda_{n-1}\cup\{\lambda_n\}$,记录找到的字典矩阵中的重建原子集合

步骤 3:由遗传算法优化得到:

$$\hat{\alpha i}_n=\mathrm{argmin}_{\alpha i}\|y-\sum_{i=1}^{N}D_n\alpha^i\|_2;$$

步骤 4:更新残差 $R^nf=y-\sum_{i=1}^{N}D_n\hat{\alpha}_n^i$,$n\leftarrow n+1$;

步骤 5:判断是否满足 $n>K$,若满足,则停止迭代;若不满足则返回步骤 1.

3 实验与分析

实验部分分别采用本文算法、Kalman 滤波方法、平滑滤波方法对核脉冲信号进行处理,比较上述三种方法的信号提取效果.利用 Matlab 仿真产生 1s 时间长度的核脉冲信号,采样频率为 1KHz,分别利用改进 OMP 算法、Kalman 滤波法、平滑滤波法对仿真脉冲信号进行处理.在遗传优化过程中,交叉率 P_c 和变异率 P_m 的大小对遗传算法的运行性能有较大的影响,本文实验部分 P_c 取为 0.5,P_m 取为 0.01,种群大小取为 20.

图 1 为 3 种不同方法在核素脉冲仿真信号上的提取结果,(a)为原始脉冲信号,(b)为 Kalman 滤波结果,(c)为平滑滤波算法结果,(d)为改进的 OMP 算法信号提取结果.对比(a)和(b)可知,Kalman 滤波法幅度误差较小,但是发生了明显的相位延迟;对比(a)和(c)可知,经过平滑滤波后的信号幅度发生了明显的削减;对比(a)和(d)可以看到,改进的 OMP 算法既保持了信号的幅度信息,也保持了其相位信息,具有较好的脉冲信号提取效果.

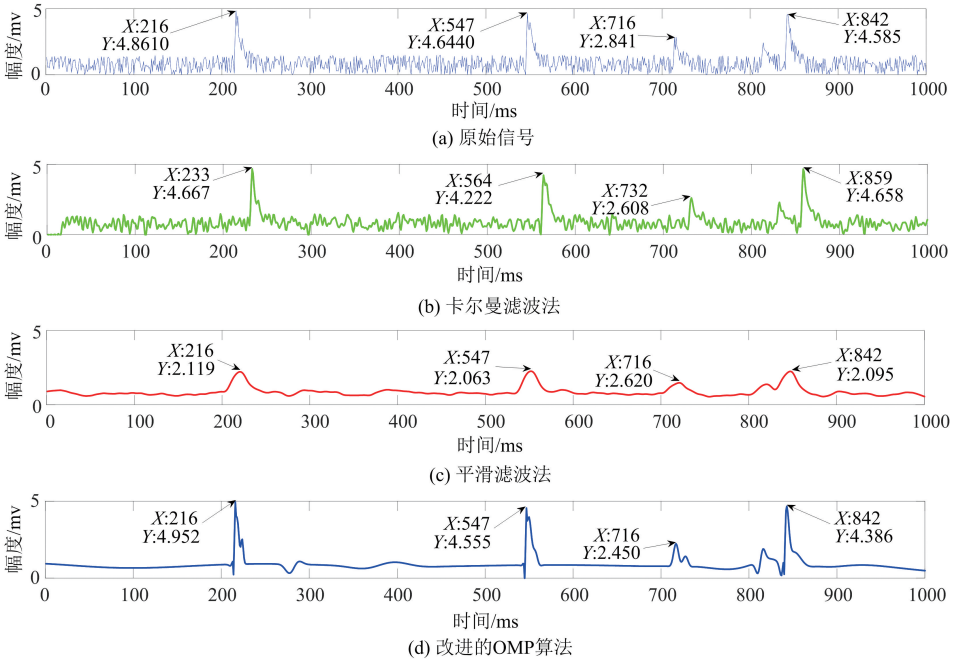

图 1 Kalman 滤波法、平滑滤波法、改进 OMP 算法对脉冲信号进行重构

Fig.1 Pulse signal reconstruction by using Kalman filtering, smooth filtering and improved OMP algorithm

图 2 对比了上述 3 种方法的信号重构效果，对比可知，Kalman 滤波法、平滑滤波法和改进的 OMP 算法在噪声信号重构过程中，随着信号信噪比的提升，重构误差都会减小.总体而言，平滑滤波法的重构误差是 3 种方法中最大的，信号重构效果最差，改进的 OMP 算法在 3 种方法中表现最优，其重构误差最小.从重构误差的角度而言，改进的 OMP 算法在核脉冲信号提取中效果最好.

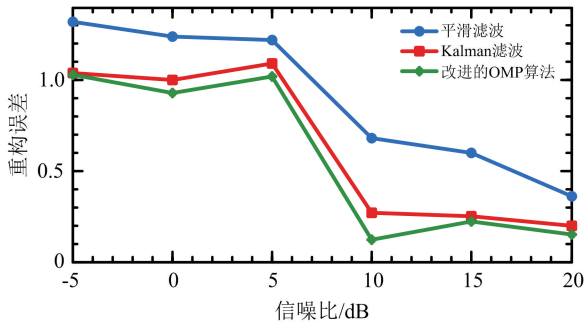

图 2　三种重构方法误差对比

Fig.2　Comparison of errors of three reconstruction algorithms

4　结论

本文采用稀疏表示模型对采集信号进行建模，并设计了一种基于 K-SVD 的稀疏表示字典构建方法，消除了探测器和噪声引起的和单脉冲信号表示字典的差异.针对非凸目标函数的优化问题，采用遗传算法改进了 OMP 算法，并最终实现了微弱核辐射脉冲信号的重构，仿真结果表明，本文方法在核脉冲信号提取方面效果明显优于传统的 Kalman 滤波和平滑滤波法，具有较小的重构误差且无相位延迟.

参考文献(References)

[1] 曾晨浩，冯孝杰，段中山，等. 基于模极大值法的 γ 能谱数据处理与分析[J]. 原子能科学技术，2017，51(7)：1305-1310.

[2] 向清沛. 基于序贯贝叶斯分析的放射性核素快速识别方法研究 [D].北京：中国工程物理研究院，2014.

[3] 李伦辉，何剑锋，王芹，等. 改进小波阈值方法对 γ 能谱去噪的研究 [J]. 原子能科学技术，2016，50(7)：1279 -1283.
LI L H，HE J F，WANG Q，et al. Study of γ energy spectrum denoising-based on improved wavelet threshold method [J]. Atomic Energy Science and Technology，2016，50(7)：1279-1283.

[4] 高晋占. 微弱信号检测 [M]. 北京：清华大学出版社，2011.

[5] 王坤朋，柴毅，苏春晓，等. 新型微弱受激散射光能量信号检测方法 [J]. 中国激光，2013，40(3)：204-209.
WANG K P，CHAI Y，SU C X，et al. Novel method for detection of weak stimulated scattering light energy signal [J]. Chinese J. Lasers，2013，40(3)：204-209.

[6] MARTIN A，HARBISON S A. Radiation Detection and Measurement[M]. Proc. IEEE，2010.

[7] WANG K，CHAI Y，SU C. Sparsely corrupted stimulated scattering signals recovery by iterative reweighted continuous basis pursuit [J]. Rev. Sci. Instrum.，2013，84(8)：339-624.

[8] MARSHALL A，OLKIN I. Sparse Representation [M]. Springe，2014.

[9] MALLAT S G，ZHANG Z. Matching pursuits with time-frequency dictionaries [J]. IEEE Transactions on Signal Processing，1993，41(12)：3397-3415.

[10] AHARON M，ELAD M，BRUCKSTEIN A. K-SVD：An algorithm for designing overcomplete dictionaries for sparse representation [J]. IEEE Transactions on Signal Processing，2006，54(11)：4311-4322.

[11] PATI Y C，REZAIIFAR R，KRISHNAPRASAD P S. Orthogonal matching pursuit：recursive function approximation with applications to wavelet decomposition [C]// The Twenty-Seventh Asilomar Conference on Signals，Systems and Computers. Pacific，USA：IEEE Press，1993：40-44.

[12] EDOARDO A，VIGGO K. On the approximability of minimizing nonzero variables or unsatisfied relations in linear systems [J]. Theoretical Computer Science，1998，209(1-2)：237-260.

[13] ENGAN K，AASE S O，HAKON H. Method of optimal directions for frame design [C]// IEEE International Conference on Acoustics，Speech，and Signal Processing. Phoenix，USA：IEEE Press，1999：2443-2446.

[14] PEI S C，DING J J. Relations between gabor transforms and fractional fourier transforms and their applications for signal processing [J]. IEEE Transactions on Signal Processing，2007，55(10)：4839-4850.

[15] LESAGE S，GRIBONVAL R，BIMBOT F，et al. Learning unions of orthonormal bases with thresholded singular value decomposition [C]// IEEE International Conference on Acoustics，Speech，and Signal Processing，2005，293-296.

[16] CHEN S S，DONOHO D L，SAUNDERS M A. Atomic decomposition by basis pursuit [J]. Society for Industrial and Applied Mathematics Philadephia，USA：IEEE Press，1998，43(1)：129-159.

文章编号:0253-2778(2018)09-0696-07

A high-speed voltage-mode sense amplifier for SRAM

LIU Kangsheng[1], YU Zhiguo[1*], WANG Tian[1], LIANG Sisi[2], QIAN Liming[2], GU Xiaofeng[1]

(1. *Department of Electronic Engineering, Jiangnan University, Wuxi* 214122, *China*;
2. *China Electronic Technology Group Corporation No.58 Research Institute, Wuxi* 214035, *China*)

Abstract: This paper reports a novel sense amplifier (SA) suitable for voltage sensing in the read operation of static random access memory (SRAM). Contrary to the conventional cross-coupled SA, an NMOS cross coupling amplifier is added as the second stage amplifier and the pull-up and pull-down circuits are added as the output circuit. The proposed structure can quickly amplify the bit line voltage difference with high gain, improve the sensitivity, and ensure that the data output port of the SRAM encounters no interference when the utility model is not working. The simulation results show that this design reduces 95% of the voltage required for the bit lines to guarantee the full swing at output nodes and shortens 80% of the sensing delay for the same input voltage difference compared with the conventional SA.

Key words: sense amplifier; cross-coupled; voltage-mode; high-speed

CLC number: TN722 **Document code**: A doi:10.3969/j.issn.0253-2778.2018.09.002

2010 Mathematics Subject Classification: 94B15

Citation: LIU Kangsheng, YU Zhiguo, WANG Tian, et al. A high-speed voltage-mode sense amplifier for SRAM[J]. Journal of University of Science and Technology of China, 2018,48(9):696-702.
刘康生,虞致国,王恬,等. 一种应用于SRAM中的高速电压模型灵敏放大器[J]. 中国科学技术大学学报,2018,48(9):696-702.

一种应用于SRAM中的高速电压模型灵敏放大器

刘康生[1],虞致国[1*],王　恬[1],梁思思[2],钱黎明[2],顾晓峰[1]

(1.江南大学电子工程系,江苏无锡 214122;2.中国电子科技集团公司第五十八研究所,江苏无锡 214035)

摘要:设计了一种应用于静态随机存储器(SRAM)读数据过程中的电压型灵敏放大器(SA).与传统交叉耦合结构SA相比,增加了由NMOS管构成的第二级交叉放大电路及由上拉和下拉电路组成的输出电路.改进的结构能在快速而且高增益地放大位线上电压差的同时,改善灵敏度低的问题,确保了SRAM在不工作时数据输出端口的输出不受内部干扰.仿真结果表明,与传统结构相比,本设计减少了为确保输出节点全摆幅而所需的95%的位线上电压,同时在相同差分电压输入的情况下,响应时间减少了80%.

关键词:灵敏放大器;交叉耦合;电压模型

Received: 2017-10-27; **Revised**: 2017-04-29

Foundation item: Supported by Fundamental Research Funds for the Central Universities (JUSRP51510), Summit of the Six Top Talents Program of Jiangsu Province (2013-DZXX-027), Postgraduate Research & Practice Innovation Program of Jiangsu Province (KYLX16_0776, SJLX16_0500, SJCX17_0510), and China Scholarship Council(201706795031).

Biography: LIU Kangsheng, male, born in 1992, Master candidate. Research field: IC design and test. E-mail: 562490958@qq.com

Corresponding author: YU Zhiguo, PhD/associate professor. E-mail: yuzhg@139.com

0 Introduction

Static random access memory (SRAM) is one of the most vital components in very large scale integration (VLSI). The memory periphery circuitry of SRAM, such as the input buffer, row decoder, column decoder, sense amplifier (SA), memory cell and output buffer, can seriously affect the overall system performance in terms of power dissipation and speed[1-2]. The SA is used to retrieve the data stored in the memory by amplifying the small voltage between two bit lines (ΔV_{BL}) to a full swing data state. Nowadays, the SA has become one of the bottlenecks for reading access time, which is an important performance parameter of SRAM[3-4].

As shown in Fig. 1, the conventional cross-coupled SA has several advantages including high speed and small silicon area[5]. However, it is not very suitable for SRAM because a high ΔV_{BL} is required on the bit lines (BL, BLB) to guarantee the full swing at output nodes[6]. In addition, the conventional crossed-coupled SA cannot achieve the completely full swing at output nodes because it has at least one DC path when the SA is in the sense mode[7]. Therefore, designing an SA with better performance based on the conventional cross-coupled one is highly valuable.

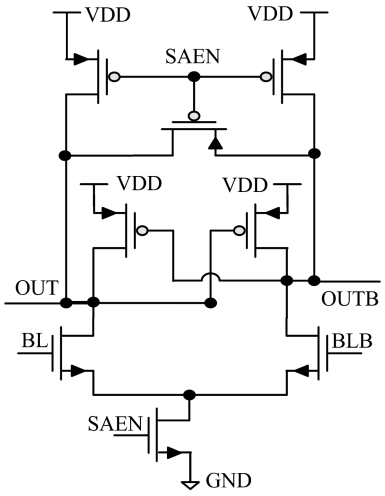

Fig.1 Conventional cross-coupled SA

A number of studies have been devoted to decreasing the sensing delay of the SA in recent years[8-11]. Ref.[8] proposed a full current-mode SA, whose sensing delay is 0.39 ns. But the full current-mode SA power consumption is 0.29 mW, which is greater than the conventional SA. Ref.[9] proposed an SA implemented in 0.13 μm technology, whose sensing delay is 1.9 ns with a power supply voltage of 1.2 V. Ref.[10] proposed an SA implemented using a 65 nm CMOS technology process, whose sensing delay and power dissipation is 2 ns and 0.018 mW. Ref.[11] exhibits 39% improvement in the sensing delay and 6.5% improvement in the offset voltage at the supply voltage of 1.0 V when compared to the conventional SA. However, the sensing delay is very important in the high speed SRAM and yet little research has been devoted to decreasing the sensing delay as much as possible.

This paper will describe the design containing two cross-coupled NMOS and two cross-coupled PMOS transistors, which decreases 80% of the sensing delay compared to the conventional SA. In this paper, we propose a modified cross-coupled SA with a smaller ΔV_{BLmin} (the minimum ΔV_{BL} required for the full swing of output signals) and a shorter sensing delay time for SRAM. The circuit structure and operation process of the proposed SA are discussed in detail in Section 1. The simulation results based on an SMIC 0.13 μm CMOS process are analyzed in Section 2, and a brief conclusion is drawn in Section 3.

1 Proposed SA

1.1 Description of the proposed SA

Fig. 2 shows the circuits of the proposed SA, including the PMOS cross-coupled circuit, the NMOS cross-coupled circuit, the pre-charging and balance circuit, and the output circuit. The PMOS circuit includes two cross-coupled PMOS transistors. The NMOS circuit includes two cross-coupled NMOS transistors. The PMOS cross-coupled circuit is activated first to amplify the small sense signal BL and BLB, and the NMOS

cross-coupled circuit shifts signals from the PMOS cross-coupled circuit closer to the logic signals. The pre-charging and balance circuit includes 6 PMOS transistors, in charge of pulling up and balancing voltages of the two levels of amplifier output ports to VDD and cutting off the output pathway. The output circuit converts the differential signals into a single signal and drives the post stage digital circuit.

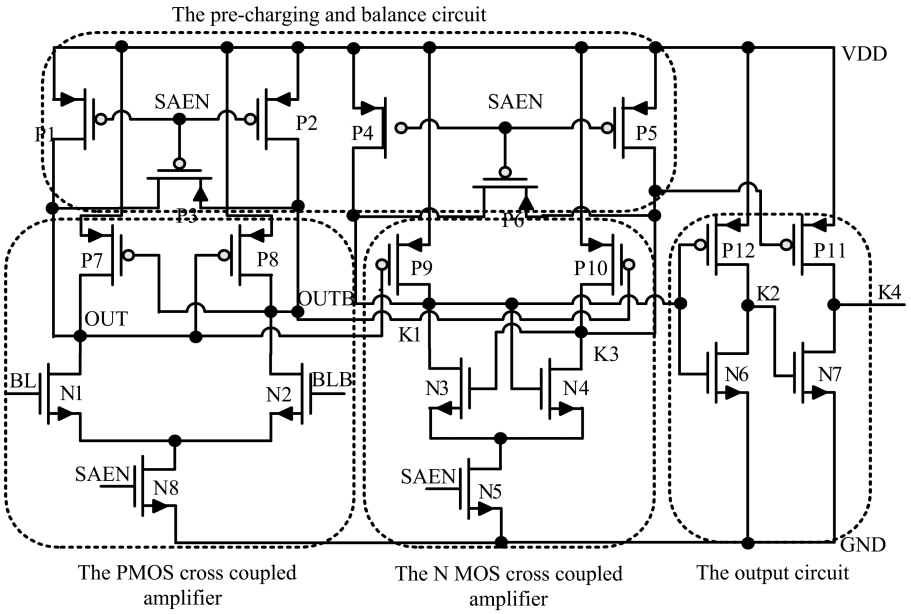

Fig.2 Circuit of the proposed cross-coupled SA

1.2 Operation of the proposed SA

The pre-charging and evaluation phase of the circuit operation are described as follows.

In the pre-charging phase, the sensing signal (SAEN) is low, so the transistors N5 and N8 are in the cut-off region. The output nodes (K4) and GND are isolated, thus no current flows from the bit lines to the output nodes. The six pre-charging transistors P1-P6 charge and balance the output nodes (OUT, OUTB, K1 and K3) to VDD, so the output pathway is cut off to ensure that the output signals of the SRAM are correct during idle time.

In the evaluation phase, the sensing signal (SAEN) is high, and ΔV_{BL} is greater than or equal to ΔV_{BLmin}. Then the pre-charging and balance circuit stops working, and the two-level amplifier circuit begins to work. When the voltage of the bit line (BL or BLB) is sampled successfully and amplified by the first PMOS cross-coupled amplifier circuit, the signals (OUT, OUTB) propagate to the second stage of the amplifier circuit and are amplified again. For the two PMOS transistors, P9 and P10, one is turned on because of the low voltage and the other is cut-off due to the high voltage. In this paper, P9 is assumed to be turned on, so P10 is cut off. When P9 is turned on , as the source is connected to the power supply VDD, the drain K1 is pulled up. The N3 transistor is turned on and its source K3 is pulled down to the logic 0, since the N5 transistor is turned on and the P10 transistor is cut off at the same time. Meanwhile, the N6 transistor is cut off , the drop-down path of K1 is cut off, and the circuit only retains the pull-up path for the K1 port, so the K1 port is pulled up to VDD by P9. Finally, the voltages at the K1 port and K3 port can be closer to logic 1 and 0 than the output voltages of the first PMOS cross-coupled amplifier circuit (OUTB, OUT), respectively.

1.3 Analysis of the proposed SA

In the evaluation phase, the proposed SA only needs one of the two PMOS transistors (P9 and P10) in the saturation state and the other in the cut-off state. This means that as long as the

voltage between the output node (OUT or OUTB) and VDD is close to the threshold voltage of P9 or P10, the proposed SA can amplify the small input signals to a completely full swing data state. So the demand for ΔV_{BL} is reduced compared to the conventional structure, meaning that the less time required to enable the word line. This can be understood by the following simple equation:

$$T \cong \frac{C_L \times \Delta V_{BL}}{I_D} \tag{1}$$

where T is the time for the bit lines being completely discharged, C_L is the capacitance loaded on the differential lines, and I_D is the current flow from bit lines. When other parameters do not change and ΔV_{BL} decreases, T is reduced, and the sensing speed increases. The simulation results are presented in the next section.

2 Simulation results and comparison

The simulations are based on a SMIC 0.13 μm CMOS process. The simulation typical corner works at 27 ℃ and 1.2 V power voltage and uses typical models. The simulation slow corner works at 125 ℃ and 1.08 V power voltage and uses slow models, and the simulation fast corner works at −45 ℃ and 1.32 V power voltage and uses fast models. The two 0.5 pF capacitances are loaded on both the bit lines respectively. The output loading of the SA is a couple of inverters. The sensing control signal is indicated by SAEN. NOUT and NOUTB are the output voltages of the proposed SA, and COUT and COUTB are the output voltages of the conventional SA. VBL and VBLB are voltages of the two bit lines, respectively.

Under the above described simulation conditions, the output voltages of both the proposed and conventional SAs with different ΔV_{BL} are shown in Fig. 3. When V_{BL} is kept at 1.2 V and V_{BLB} increases gradually, the ΔV_{BL} decreases obviously. We can find that the output voltages of the conventional SA are kept away from the logic 1 and 0 gradually with decreasing ΔV_{BL}. However, the output voltages of the proposed SA (NOUTB, NOUT) are kept around 1.2 V and 0 V even when the ΔV_{BL} is reduced to 0.03 V. At the same state, COUT and COUTB are 0.8995 V and 0.3092 V, respectively. The ΔV_{BLmin} of the proposed SA is reduced by 95% compared with the conventional one.

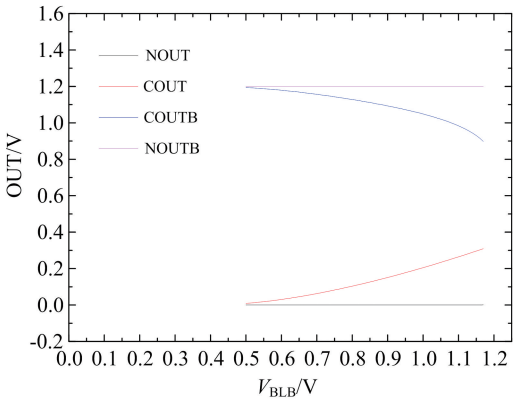

Fig.3 Output voltages of both the proposed and conventional SAs with different ΔV_{BL}

Fig.4 shows the simulation waveforms of both the proposed and conventional SAs with different ΔV_{BL}. The ΔV_{BL} changes from 700 mV to 100 mV for typical corners. As shown in Fig. 4, the sensing delay of both the proposed and conventional SAs are 0.68ns and 1.5 ns, respectively. The sensing delay of the proposed SA is reduced by 80% compared with the conventional one.

The comparison results of average power current, indicative of the average power consumption of both the proposed and conventional SAs for typical corners are shown in Fig. 5. The simulation results show that average power consumption of both the proposed and conventional SAs are 0.072 mW and 0.024 mW, respectively. The conventional SA exhibits less power current than the proposed one with the same ΔV_{BL} because there is an additional DC path in the proposed SA at the evaluation phase. However, the reduced bit-line swing can save the whole SRAM energy. When the ΔV_{BL} is less than about 60 mV, the increasing speed of average power current is faster. Thus the suitable ΔV_{BLmin} for the proposed SA is 60 mV, there is an additional DC path in the proposed SA at the evaluation phase. However, the reduced bit-line swing can save the whole SRAM energy. When

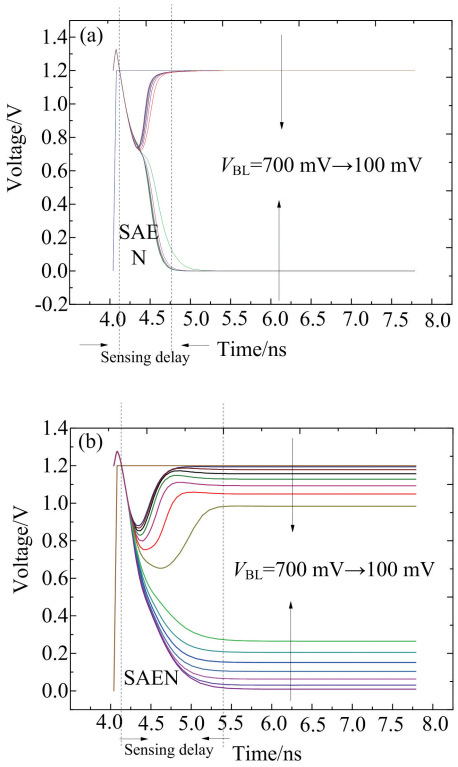

Fig.4 Simulation waveforms of both the proposed (a) and conventional SAs (b) with different ΔV_{BL}

the ΔV_{BL} is less than about 60 mV, the increasing speed of average power current is faster. Thus the suitable ΔV_{BLmin} for the proposed SA is 60 mV.

Fig. 6 (a) shows the power current simulation

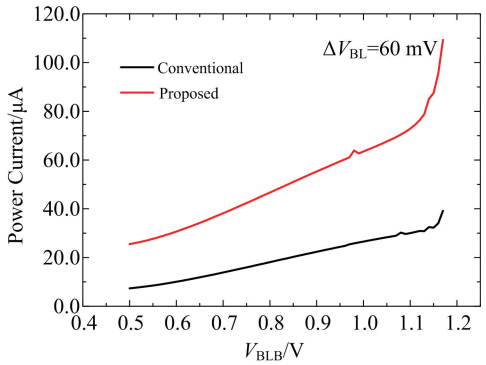

Fig.5 Power current of both the proposed and conventional SAs with different ΔV_{BL}

waveforms of the proposed SA for typical, fast and slow corners when ΔV_{BL} = 100 mV. Fig. 6 (b), (c), (d) show the output voltage simulation waveforms of the proposed and conventional SAs for typical, fast and slow corners when ΔV_{BL} = 100 mV, respectively. The results indicate that the proposed SA can work normally at the three corners. For the fast corner, the power current is greater than that of the typical corner by 150 μA and the speed is faster than that of the typical corner by 0.2 ns. For the typical corner, the power current is 120 μA greater than that of the slow corner by 120 μA and the speed is faster than that of the slow corner by 0.8 ns.

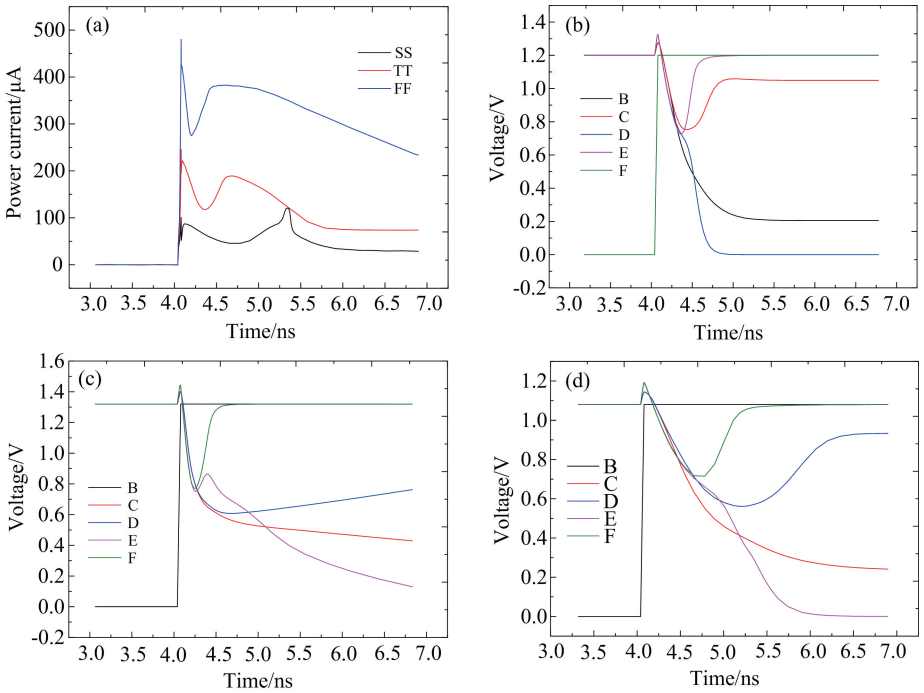

Fig.6 (a) Power current of the proposed SA for SS, TT and FF PVT corners, the output voltages of both the proposed and conventional SAs for (b) TT, (c) FF, and (d) SS PVT corners